<u>Claims</u>

1. A method for executing a simulation of a hardware device, the method comprising the steps of:

    providing at least one update object having update initialization criteria;

    providing at least one hardware object simulating functionality associated with at least one hardware device, the at least one hardware object being responsive to the at least one update object;

    providing at least one master object in communication with the at least one update object and the at least one hardware object;

    advancing, by the master object, the at least one update object by a predetermined increment; and

    executing the at least one hardware object based at least in part on the incremented update object.

2. The method of claim 1 wherein the update object comprises a clock object.

3. The method of claim 1 wherein the update object comprises a level object.

4. The method of claim 1 wherein the update object comprises an arbitrary function object.

5. The method of claim 2 wherein the update initialization criteria comprise at least one of a clock period, a clock duty cycle, a clock initial value, and a clock offset.

6. The method of claim 3 wherein the update initialization criteria comprise at least one of a level initial value and a level transition time.

7. The method of claim 4 wherein the update initialization criteria comprise a

2   predetermined value corresponding to a predetermined time.

1   8. The method of claim 1 further comprising at least one transactor object

2   associated with the hardware object.

1   9. The method of claim 1 wherein the predetermined increment varies based

2   at least in part on the at least one update object.

1   10. The method of claim 1 wherein the execution step comprises updating an

2   interconnection object in communication with the at least one hardware

3   object.

1   11. The method of claim 1 wherein the hardware object comprises coding in a

2   high-level language.

1   12. The method of claim 11 wherein the high-level language comprises at

2   least one of C, C++, SystemC, and Java.

1   13. The method of claim 1 wherein the hardware object comprises coding in

2   low-level assembly code.

1   14. The method of claim 8 wherein the transactor comprises an abstract

2   interface and a pin-level interface, the abstract interface being in

3   communication with an execution environment and the pin-level interface

4   being in communication with the hardware object.

1   15. The method of claim 8 wherein the hardware object, in communication

2   with the transactor, comprises a representation of a hardware device.

1   16. An apparatus for executing a simulation of a hardware device, the

2   apparatus comprising:

3   at least one update object having update initialization criteria;

4   at least one hardware object simulating functionality associated with at

5   least one hardware device, the at least one hardware object being

6	responsive to the at least one update object;
7	at least one master object in communication with the at least one update
8	object and the at least one hardware object, the at least one master
9	object being configured to advance the at least one update object by a
10	predetermined increment and thereby cause execution of the at least
11	one hardware object based at least in part on the incremented update
12	object.

1	17. The apparatus of claim 16 wherein the update object comprises a clock
2	object.

1	18. The apparatus of claim 16 wherein the update object comprises a level
2	object.

1	19. The apparatus of claim 16 wherein the update object comprises an
2	arbitrary function object.

1	20. The apparatus of claim 17 wherein the update initialization criteria
2	comprise at least one of a clock period, a clock duty cycle, a clock initial
3	value, and a clock offset.

1	21. The apparatus of claim 18 wherein the update initialization criteria
2	comprise at least one of a level initial value and a level transition time.

1	22. The apparatus of claim 19 wherein the update initialization criteria
2	comprises a predetermined value corresponding to a predetermined time.

1	23. The apparatus of claim 16 further comprising the at least one transactor
2	object associated with the hardware object.

1	24. The apparatus of claim 16 wherein the predetermined increment varies
2	based at least in part on the at least one update object.

1	29. The apparatus of claim 23 wherein the transactor comprises an abstract

2   interface and a pin-level interface, the abstract interface being in
3   communication with an execution environment and the pin-level interface
4   being in communication with the hardware object.

1   30. The apparatus of claim 23 wherein the hardware object, in communication
2   with the transactor, comprises a representation of a hardware device.